FIG. 1

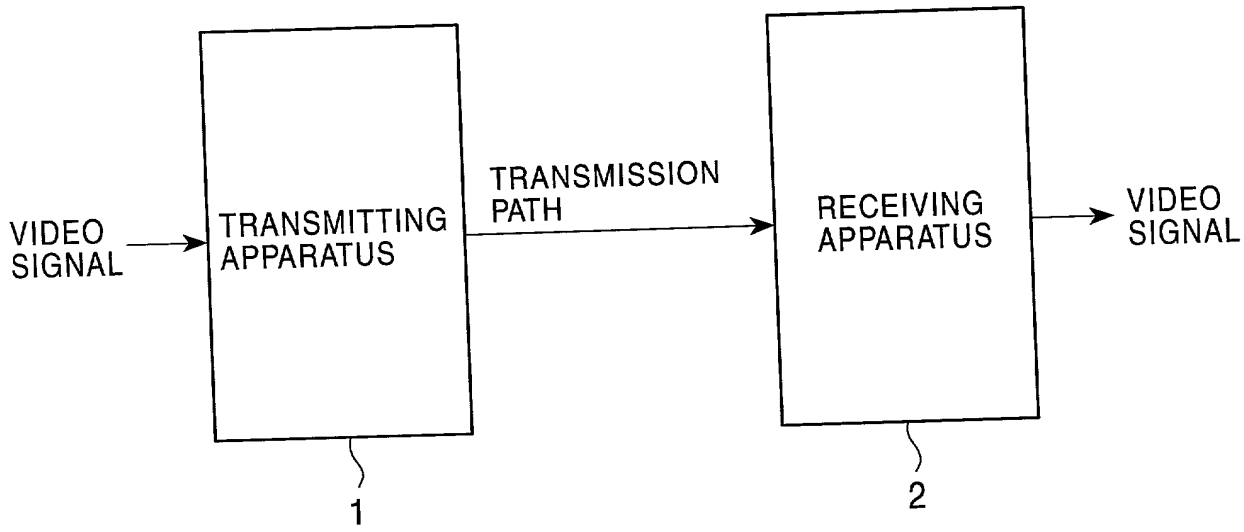

VIDEO SIGNAL
TRANSMITTING APPARATUS
TRANSMISSION PATH
RECEIVING APPARATUS
VIDEO SIGNAL
1
2

FIG. 2

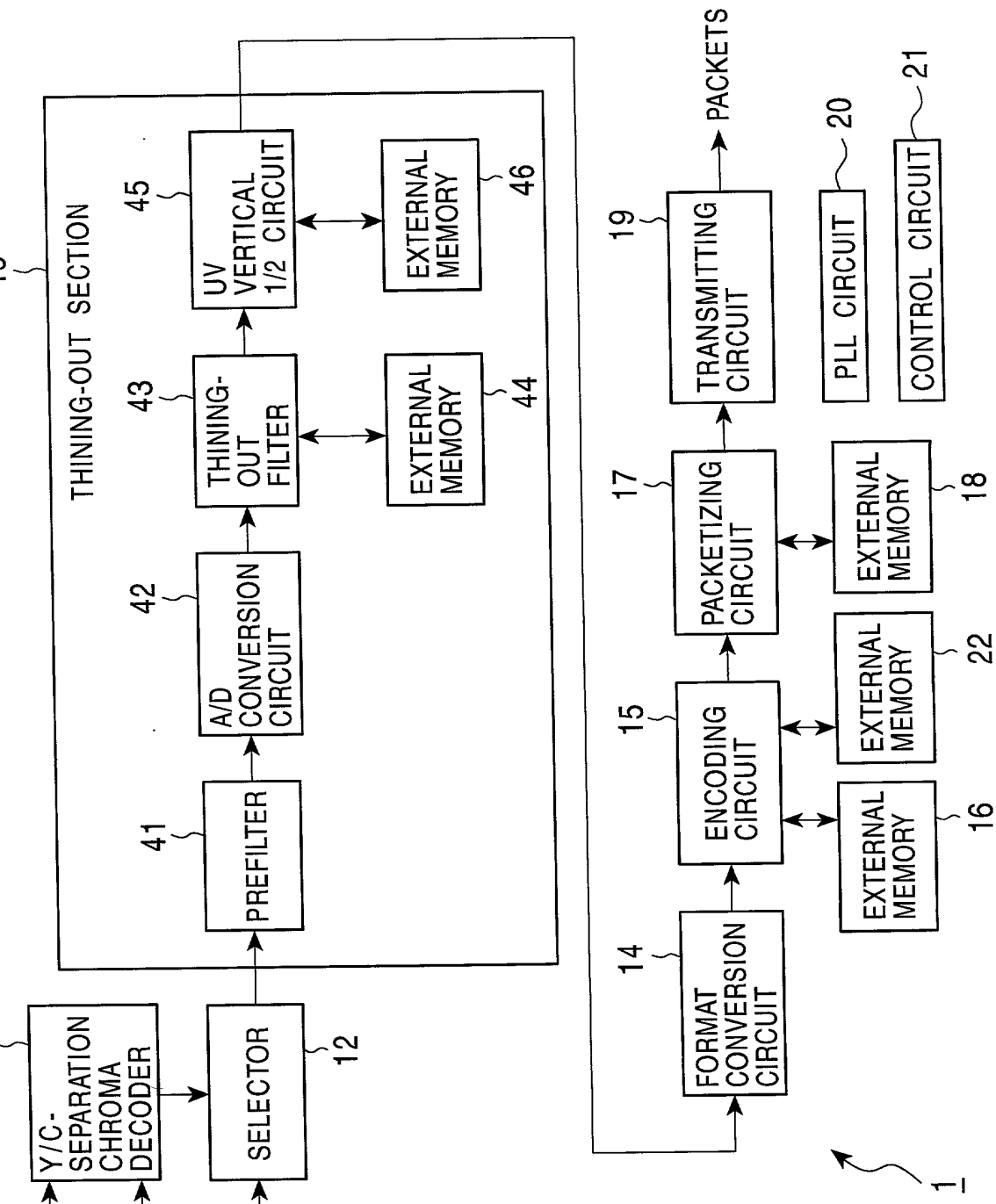

COMPOSITE VIDEO SIGNAL
Y/C SIGNALS
Y/U/V SIGNALS
11
Y/C-SEPARATION CHROMA DECODER
12
SELECTOR
13
THINING-OUT SECTION
41
PREFILTER
42
A/D CONVERSION CIRCUIT
43
THINING-OUT FILTER
44
EXTERNAL MEMORY
45
UV VERTICAL 1/2 CIRCUIT
46
EXTERNAL MEMORY
14
FORMAT CONVERSION CIRCUIT
15
ENCODING CIRCUIT
16
EXTERNAL MEMORY
17
PACKETIZING CIRCUIT
18
EXTERNAL MEMORY
19
TRANSMITTING CIRCUIT
PACKETS
20
PLL CIRCUIT
21
CONTROL CIRCUIT
22
EXTERNAL MEMORY
1

FIG. 3

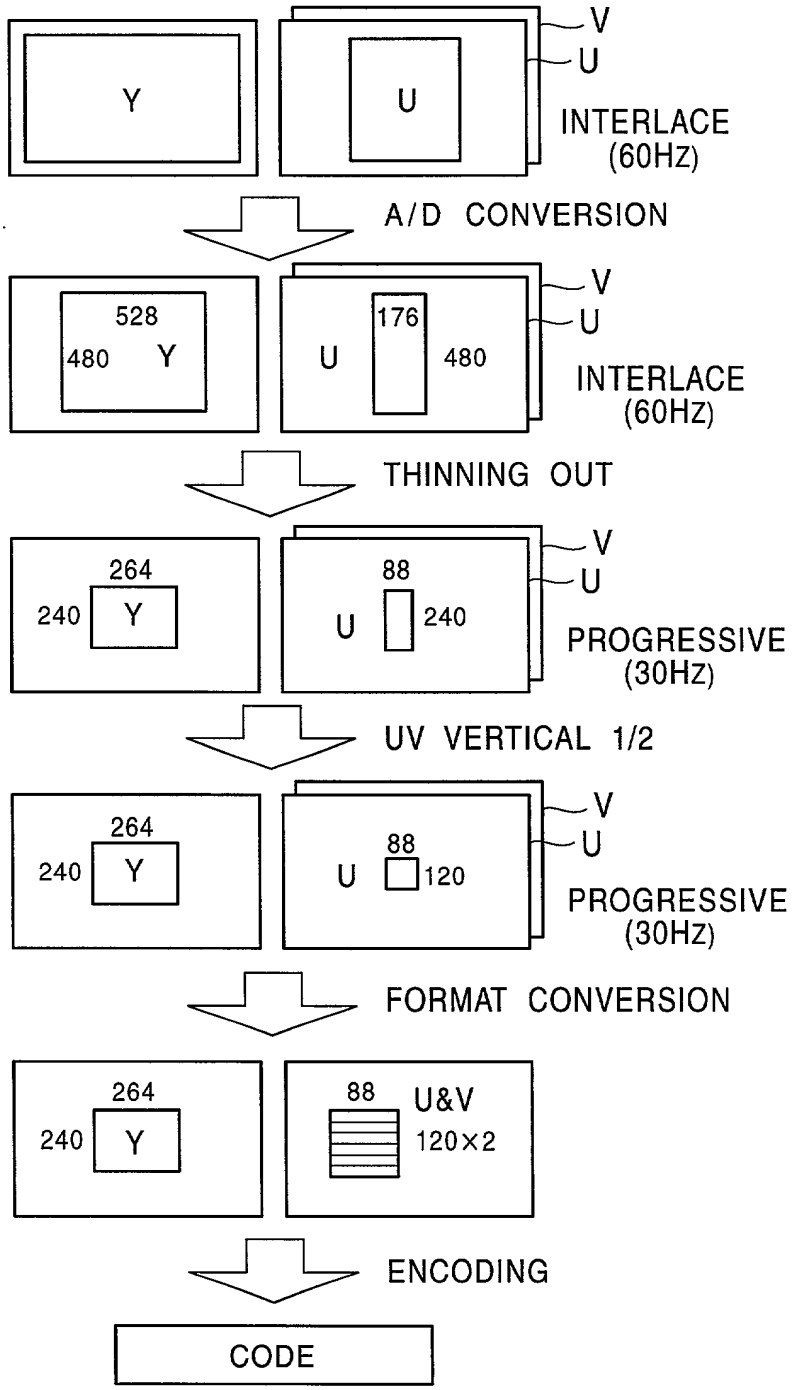

Y
U
V
U
INTERLACE
(60Hz)
A/D CONVERSION
528
480
Y
U
176
480
V
U
INTERLACE
(60Hz)
THINNING OUT
264
240
Y
U
88
240
V
U
PROGRESSIVE
(30Hz)
UV VERTICAL 1/2
264
240
Y
U
88
120
V
U
PROGRESSIVE
(30Hz)
FORMAT CONVERSION
264
240
Y
88
U&V
120×2
ENCODING
CODE

FIG. 4

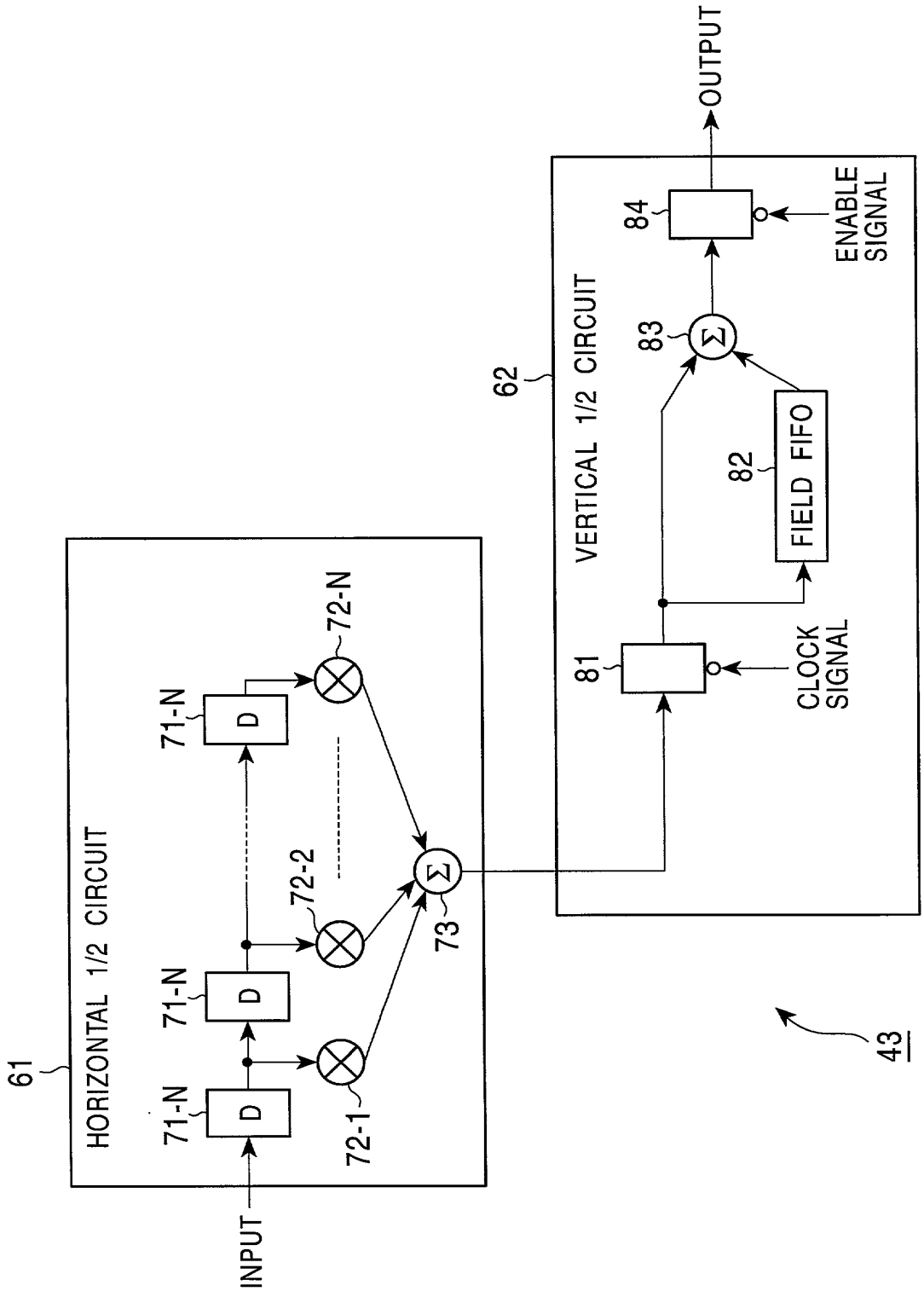

61
HORIZONTAL 1/2 CIRCUIT
INPUT
D
71-N
72-1
72-2
72-N
73
62
VERTICAL 1/2 CIRCUIT
81
82
FIELD FIFO
83
84
CLOCK SIGNAL
ENABLE SIGNAL
OUTPUT
43

FIG. 5

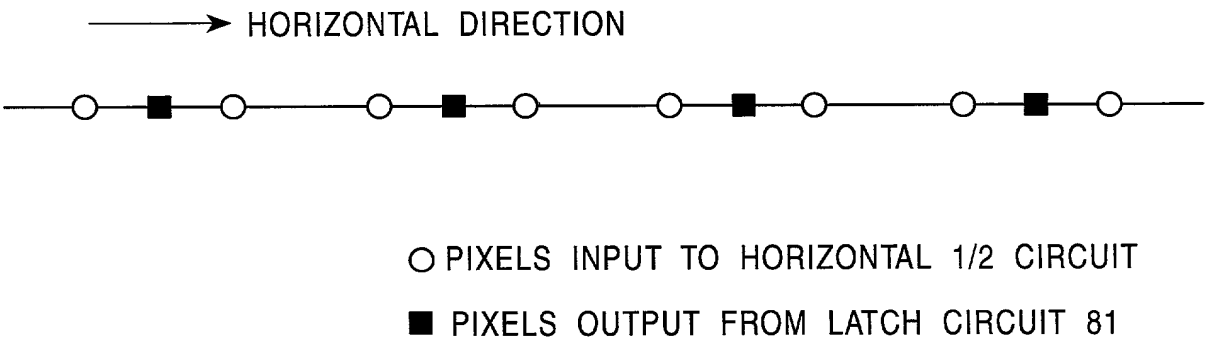
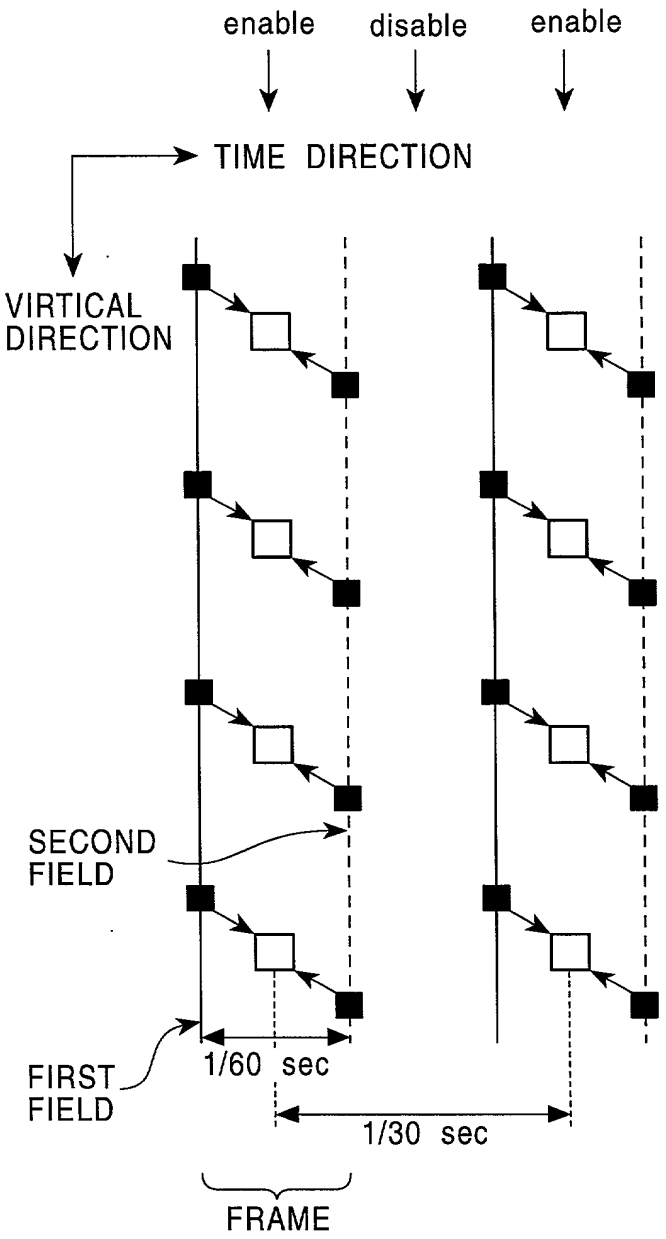

HORIZONTAL DIRECTION
○ PIXELS INPUT TO HORIZONTAL 1/2 CIRCUIT
■ PIXELS OUTPUT FROM LATCH CIRCUIT 81

FIG. 6



■ PIXELS OUTPUT FROM LATCH CIRCUIT 81

□ PIXELS OUTPUT FROM LATCH CIRCUIT 84

FIG. 7

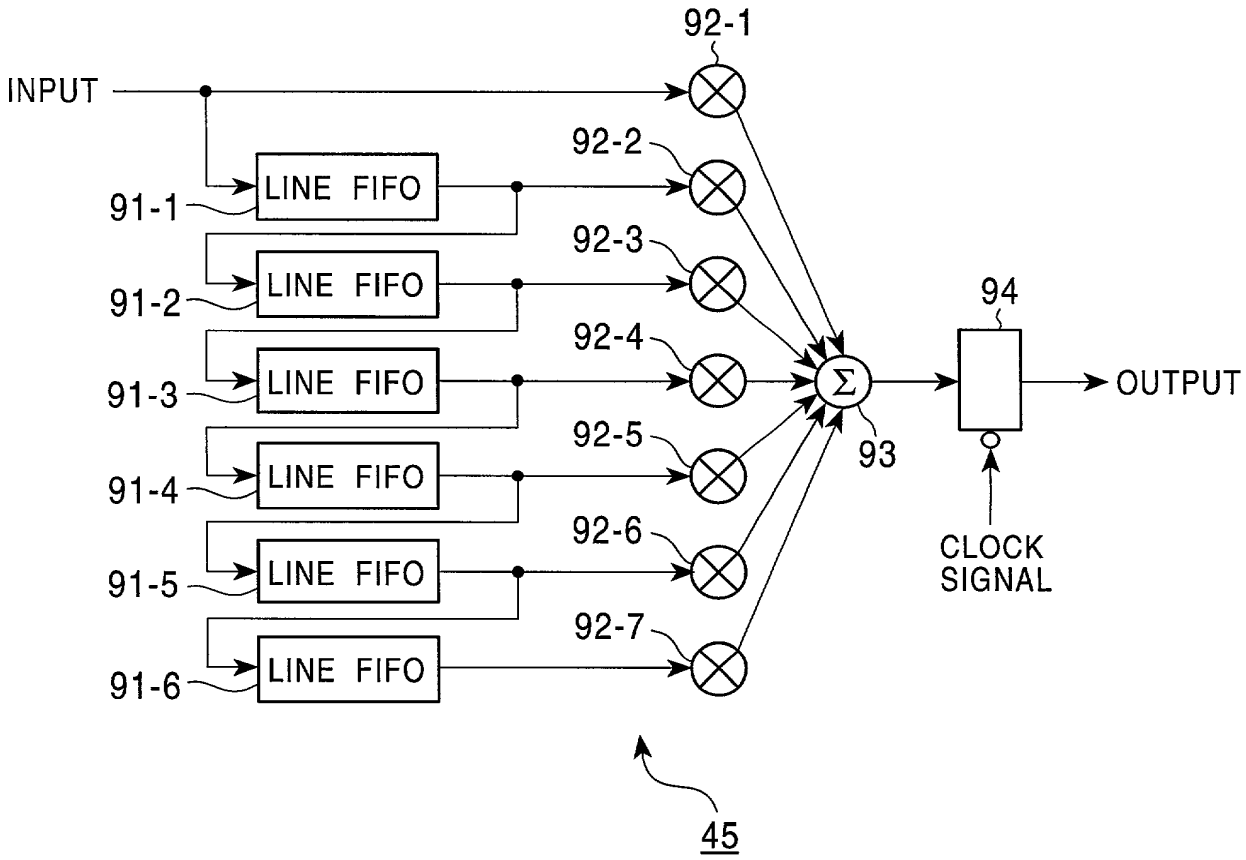

INPUT
91-1
91-2
91-3
91-4
91-5
91-6
LINE FIFO
LINE FIFO
LINE FIFO
LINE FIFO
LINE FIFO
LINE FIFO
92-1
92-2
92-3
92-4
92-5
92-6
92-7
Σ
93
94
OUTPUT
CLOCK SIGNAL
45

FIG. 8

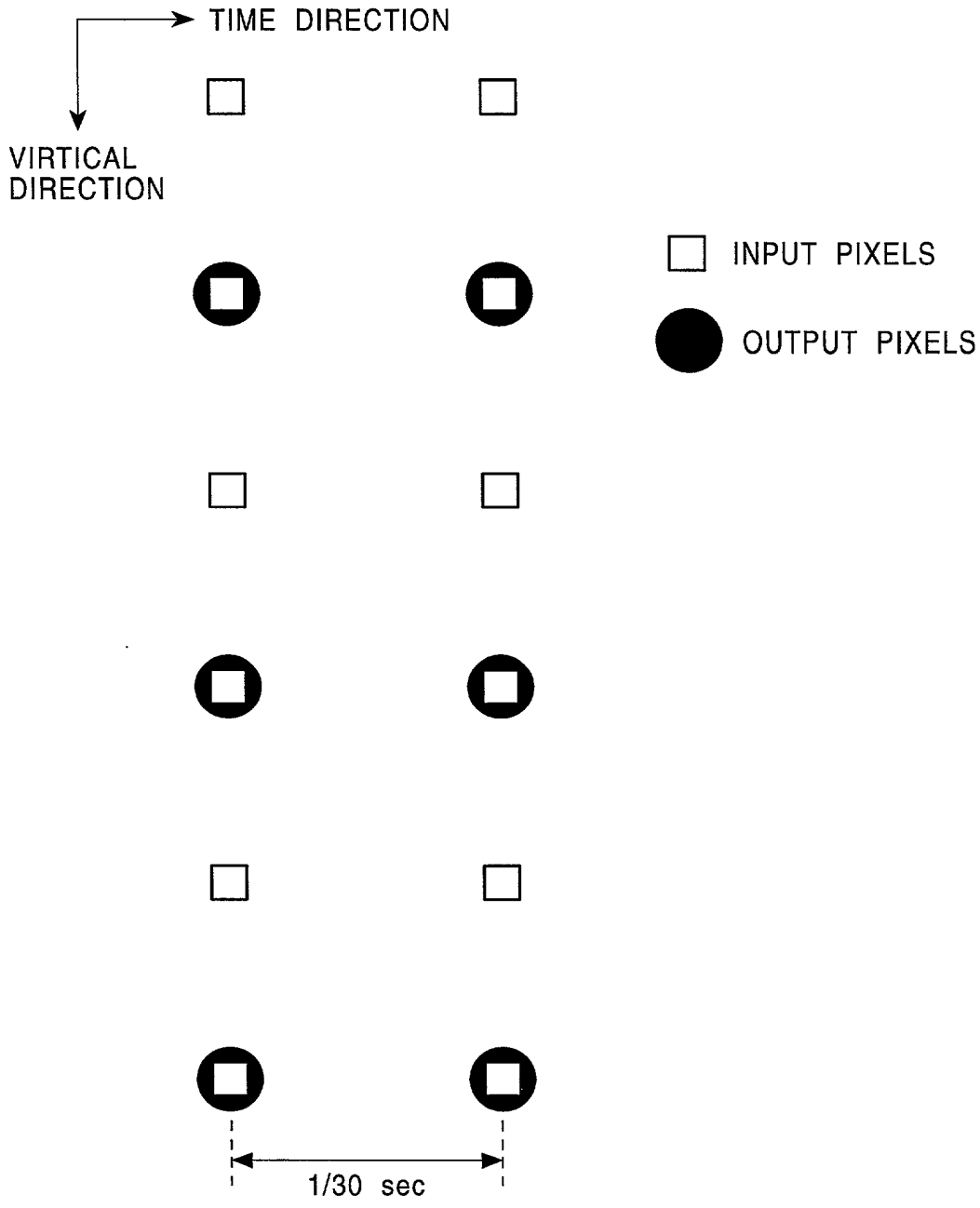

TIME DIRECTION
VIRTICAL DIRECTION
INPUT PIXELS
OUTPUT PIXELS
1/30 sec

FIG. 9

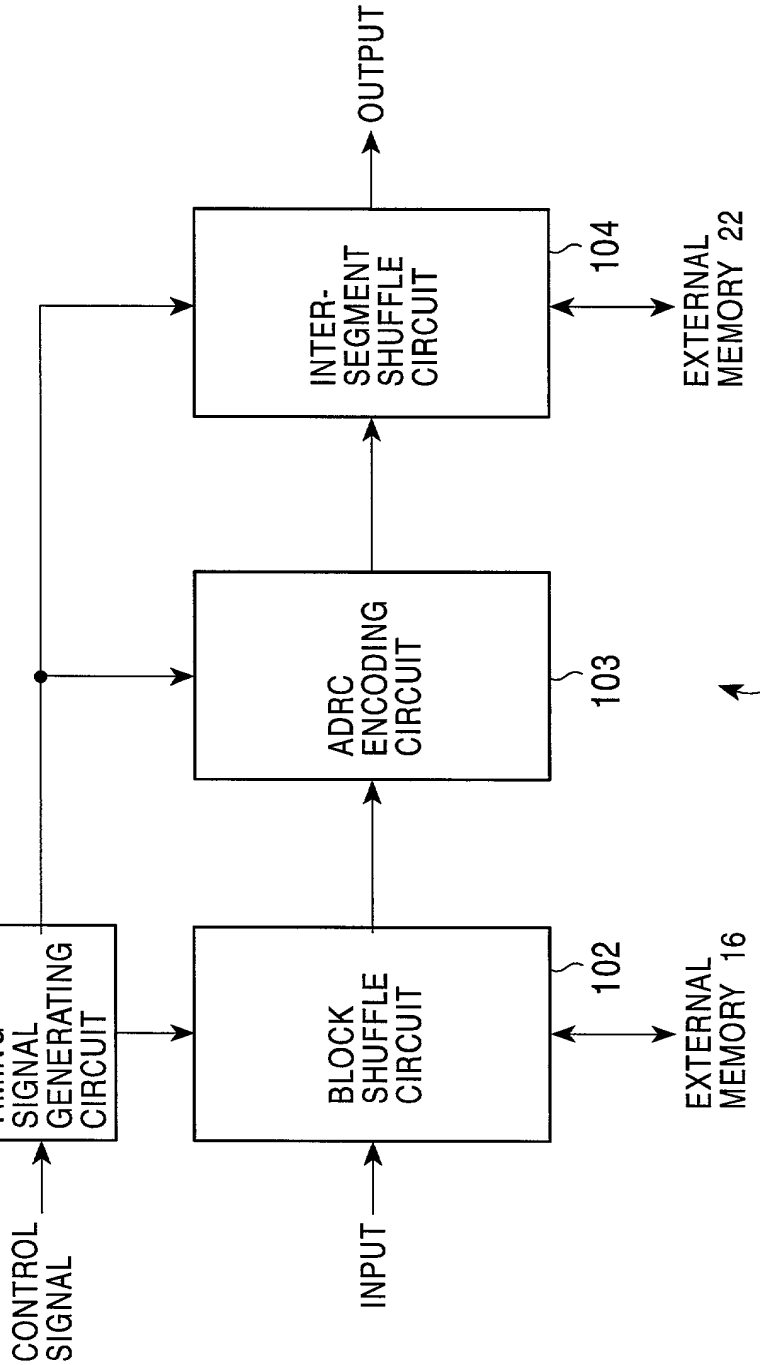

CONTROL SIGNAL
INPUT
101
TIMING-SIGNAL GENERATING CIRCUIT
BLOCK SHUFFLE CIRCUIT
102
EXTERNAL MEMORY 16
ADRC ENCODING CIRCUIT
103
INTER-SEGMENT SHUFFLE CIRCUIT
104
EXTERNAL MEMORY 22
OUTPUT
15

FIG. 10

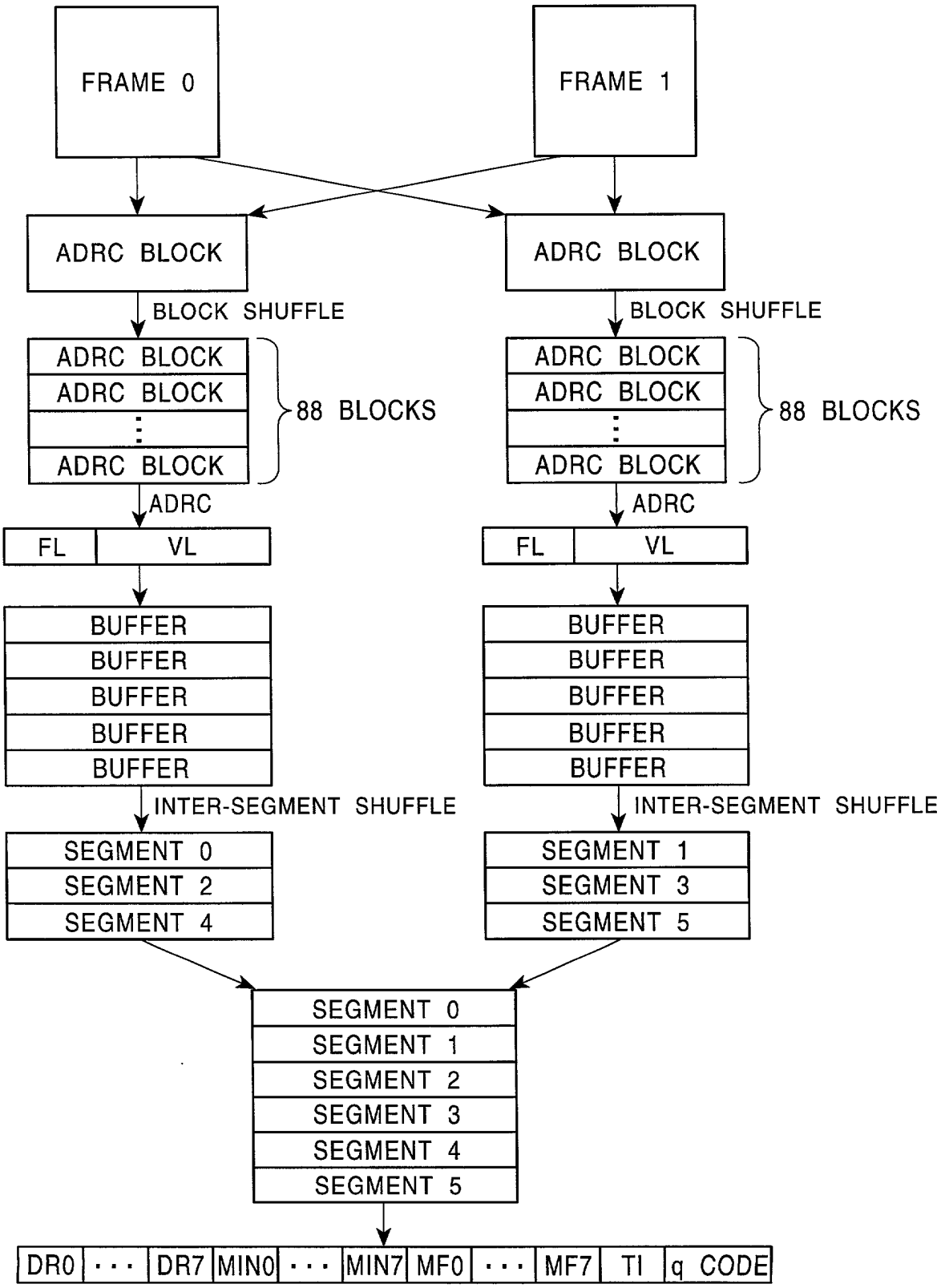
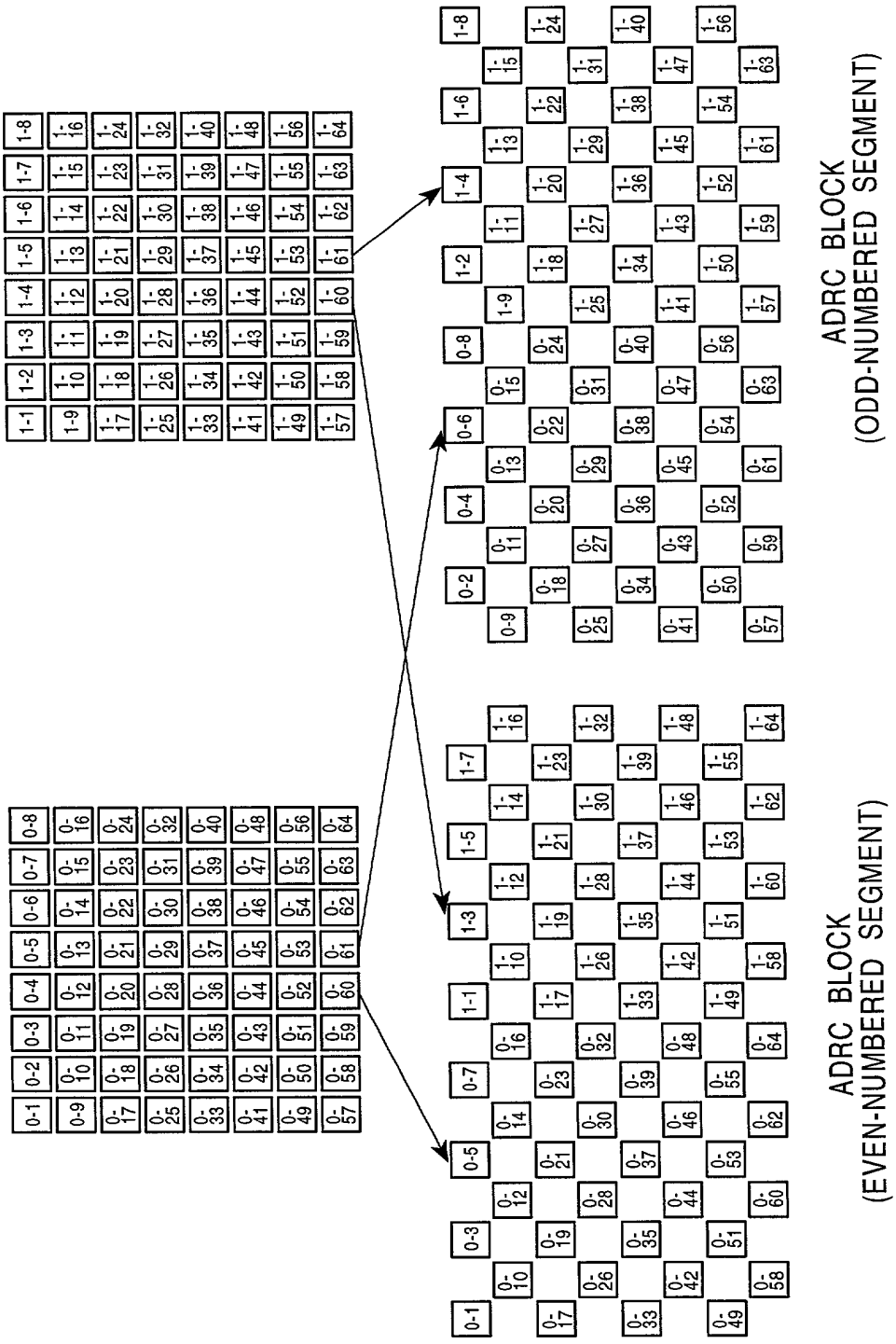

FRAME 0
FRAME 1
ADRC BLOCK
ADRC BLOCK
BLOCK SHUFFLE
BLOCK SHUFFLE
ADRC BLOCK
ADRC BLOCK
ADRC BLOCK
88 BLOCKS
ADRC BLOCK
ADRC BLOCK
ADRC BLOCK
88 BLOCKS
ADRC
ADRC
FL
VL
FL
VL
BUFFER
BUFFER
BUFFER
BUFFER
BUFFER
BUFFER
BUFFER
BUFFER
BUFFER
BUFFER
INTER-SEGMENT SHUFFLE
INTER-SEGMENT SHUFFLE
SEGMENT 0
SEGMENT 2
SEGMENT 4
SEGMENT 1
SEGMENT 3
SEGMENT 5
SEGMENT 0
SEGMENT 1
SEGMENT 2
SEGMENT 3
SEGMENT 4
SEGMENT 5
DR0
DR7
MIN0
MIN7
MF0
MF7
TI
q CODE

FIG. 11


BLOCK IN FRAME 0
CORRESPONDING BLOCK IN FRAME 1
ADRC BLOCK (EVEN-NUMBERED SEGMENT)
ADRC BLOCK (ODD-NUMBERED SEGMENT)